library IEEE;

use IEEE.STD\_LOGIC\_1164.all;

entity DMUX is

generic (n:natural:= 2);

port(

e : in BIT;

s : in BIT\_VECTOR(0 to n);

x : in BIT;

y : out BIT\_VECTOR(0 to 2\*\*(n+1)-1)

);

end DMUX;

--}} End of automatically maintained section

architecture Arhitectura of DMUX is

begin

-- enter your statements here --

process(s,x,e)

variable calculat:natural;

begin

if e='0' then

calculat:=0;

for indice in 0 to n loop

calculat := calculat \* 2 + natural'val(bit'pos(s(indice)));

end loop;

y(calculat) <= x;

for indice in 0 to 2\*\*(n+1)-1 loop

if indice/=calculat then

y(indice) <= not(x);

end if;

end loop;

else

for indice in 0 to 2\*\*(n+1)-1 loop

y(indice)<='0';

end loop;

end if;

end process;

end Arhitectura;